

REMARKS/ARGUMENT

This is responsive to the Office Action dated September 12, 2002.

The Examiner's finding of patentable subject matter in claim 41 is gratefully acknowledged. This claim has been rewritten in independent form and is therefore allowable. Claim 42 recites substantially the same features as claim 41. Claim 42 has been placed in independent form by combining it with the features of claim 29. Therefore, both claims 41 and 42 are now in condition for allowance.

Claims 29-40 were rejected as being unpatentable over Cogan et al. in view of secondary references including Harada. The Examiner cited Harada as disclosing the feature recited at claim 29, lines 12-14, namely "each of said intermediate trenches . . . being filled with a conductive polysilicon plug of said opposite conductivity type."

This rejection is respectfully traversed. Harada's trench 14 is not filled with a polysilicon plug as recited in claim 29. Rather, as explained in Harada at column 4, lines 49-58, the trench 14 contains an extension of the emitter electrode 7, which is made of "a metal such as aluminum."

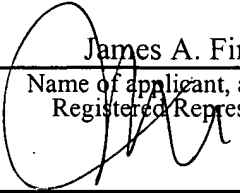
In addition, Harada is fundamentally inapplicable to the present invention. The invention is a trench MOS-gated device. Harada discloses an IGBT. These two different types of semiconductor devices have entirely different functions, requirements and behavior and the structure of the trench-type bipolar device in Harada would not be understood by a skilled individual to have any applicability to the MOS device disclosed in the primary reference, Cogan et al. For this reason as well, the rejection is traversed.

New dependent claims 45 and 46 are related to claims 41 and 42 and are allowable for at least the same reasons.

In view of the foregoing amendments and remarks, the Examiner is requested to allow claims 29-46 and pass this case to issue.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Asst. Commissioner for Patents, Washington, D.C. 20231, on December 12, 2002:

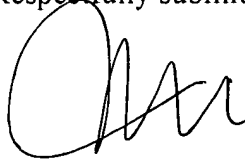
James A. Finder
Name of applicant, assignee or
Registered Representative


Signature

December 12, 2002
Date of Signature

JAF:db

Respectfully submitted,



James A. Finder
Registration No.: 30,173
OSTROLENK, FABER, GERB & SOFFEN, LLP
1180 Avenue of the Americas
New York, New York 10036-8403
Telephone: (212) 382-0700



APPENDIX B
VERSION WITH MARKINGS TO SHOW CHANGES MADE
37 C.F.R. § 1.121(b)(iii) AND (c)(ii)

CLAIMS:

(AMENDED) 34. The device of claim 29, wherein:

at least a plurality of said active trenches containing MOS gated structures are polygonal in topology and are symmetrically spaced and disposed over the surface of said silicon wafer;

said source regions surrounding respective ones of said active trenches containing a MOS gated structure;

said intermediate trenches surrounding said at least a plurality of said active trenches consisting of a trench of lattice shape in topology which extends in the space defined between spaced active trenches having said polygonal [to pology] topology.

(AMENDED) 41. [The device of claim 36,] A trench MOS gated device which has improved resistance to both high radiation and single event high energy charged particles (SEE), comprising:

a silicon wafer of one conductivity type having a plurality of spaced shallow active trenches containing respective gate structures and a plurality of intermediate trenches each disposed between a respective pair of active trenches;

each of said active trenches and each of said intermediate trenches having at least partly vertical walls joined at their bottoms by respective trench bottoms;

each of said active trenches containing a gate structure having a gate dielectric on at least portions of its said vertical walls, a bottom dielectric on the bottom and a conductive polysilicon plug of said one conductivity type which acts as a gate electrode and which contacts at least the interior surface of said gate dielectric;

each of said intermediate trenches having a shallow diffusion of a conductivity type opposite to said one conductivity type extending from its walls and bottom and being filled with a conductive polysilicon plug of said opposite conductivity type;

the spaces between said active and intermediate trenches each containing a channel region of said opposite conductivity type and an upper source region comprising a diffusion in contact with said respective polysilicon plugs in said corresponding intermediate trenches;
a common source contact contacting each of said source regions and each of said conductive plugs in each of said intermediate trenches; and
a common gate electrode connected to each of said conductive plugs in each of said active trenches containing a gate structure and a drain contact connected to a drift region beneath said active and intermediate trenches;
wherein the thickness of said gate dielectric is chosen to optimize resistance to high radiation effects and wherein the thickness of said bottom dielectric is chosen to optimize resistance to SEE; and

wherein said trench MOS gated device is supported in a die which further contains a termination structure; said plurality of active trenches and said plurality of intermediate trenches defining an active area; said termination structure comprising a plurality of concentric ring-shaped trenches surrounding said active area and extending radially from said active area toward the edge of said die; each of said plurality of ring-shaped trenches having a diffusion extending from its walls and bottom which is of said opposite conductivity type; each of said plurality of ring-shaped trenches having a conductive polysilicon plug of said opposite conductivity type; said plurality of ring-shaped trenches being out of direct contact with said source contact and comprising floating rings.

(AMENDED) 42. [The device of claim 10,] A trench MOS gated device which has improved resistance to both high radiation and single event high energy charged particles (SEE), comprising:

a silicon wafer of one conductivity type having a plurality of spaced shallow active trenches containing respective gate structures and a plurality of intermediate trenches each disposed between a respective pair of active trenches;

each of said active trenches and each of said intermediate trenches having at least partly vertical walls joined at their bottoms by respective trench bottoms;

each of said active trenches containing a gate structure having a gate dielectric on at least portions of its said vertical walls, a bottom dielectric on the bottom and a conductive polysilicon plug of said one conductivity type which acts as a gate electrode and which contacts at least the interior surface of said gate dielectric;

each of said intermediate trenches having a shallow diffusion of a conductivity type opposite to said one conductivity type extending from its walls and bottom and being filled with a conductive polysilicon plug of said opposite conductivity type;

the spaces between said active and intermediate trenches each containing a channel region of said opposite conductivity type and an upper source region comprising a diffusion in contact with said respective polysilicon plugs in said corresponding intermediate trenches;

a common source contact contacting each of said source regions and each of said conductive plugs in each of said intermediate trenches; and

a common gate electrode connected to each of said conductive plugs in each of said active trenches containing a gate structure and a drain contact connected to a drift region beneath said active and intermediate trenches;

wherein said trench MOS gated device is supported in a die which further contains a termination structure; said plurality of active trenches containing a gate structure and said plurality of intermediate trenches defining an active area; said termination structure comprising a plurality of concentric ring-shaped trenches surrounding said active area and extending radially from said active area toward the edge of said die; each of said plurality of ring-shaped trenches having a diffusion extending from its walls and bottom which is of said opposite conductivity type; each of said plurality of ring-shaped trenches having a conductive polysilicon plug of said opposite conductivity type; said plurality of ring-shaped trenches being out of direct contact with said source contact and comprising floating rings.